REMARKS

Reconsideration of the above-identified application in view of the foregoing amendments and following remarks is respectfully requested.

A. Claim Status / Explanation of Amendments

Claims 1-19 were pending of which claims 1-13 were rejected, claims 1-3, 5, and 7-8 were objected to, and claims 14-19 were withdrawn from consideration as a result of a previous restriction requirement. Applicants reserve the right to pursue withdrawn claims in a divisional application. As to matters of form, claims 1-13 were rejected pursuant to 35 U.S.C. § 112, second paragraph as allegedly being indefinite. [11/16/07 Office Action, p. 4]. Claims 1-2 and 5 were also objected to as allegedly providing insufficient antecedent basis for the recitation of multiple "regions" in claims 1-2 and of multiple "gate electrodes" in claims 1 and 5. Claim 3 is objected to for reciting "MIS transistor according to claim 1 or wherein." [11/16/07 Office Action, p. 2-3].

By this paper, claims 1-3 and 5-6 are amended while claims 4 and 7-8 are canceled without prejudice or disclaimer. Applicants reserve the right to pursue canceled claims in a continuing application. The cancellation of claims 4 and 7-8 renders all rejections of and objections to these claims as moot. Claims 1 and 5 are amended such that the element "formed on a semiconductor substrate" is deleted from the preamble. Claims 1 and 5 are further amended to clarify the structure of the gate electrode and diffusion regions with corresponding changes being made to dependent claims 2-3 and 6 to correct for antecedent basis. Additional grammatical changes have been made to claim 5 to clarify the structure of the semiconductor substrate and gate insulator. Claim 3 has also been amended to correct a typographical error by deleting the word "or" in line 1. Support for the amendments to claims 1-3 and 5-6 may be

found throughout the application as originally filed including, for example, at least Figs. 6-7 and accompanying descriptive text. Applicants respectfully assert that the above amendments address each and every objection and Section 112 rejection set forth by the Office Action.

No new matter will be introduced into this application by entry of these amendments. Entry is respectfully requested.

As to the merits, claims 1-13 were rejected pursuant to 35 U.S.C. § 102(b) as allegedly being anticipated by U.S. Patent Application No. 2003/0102497 to Fried, et al. ("Fried"). [11/16/07 Office Action, p. 3]. Claims 7 and 8 were objected to under 37 C.F.R. § 1.75 as allegedly being substantial duplicates of claim 6. [11/16/07 Office Action, p. 3].

B. Claims 1-3, 5-6, and 9-13 are Not Anticipated by Fried

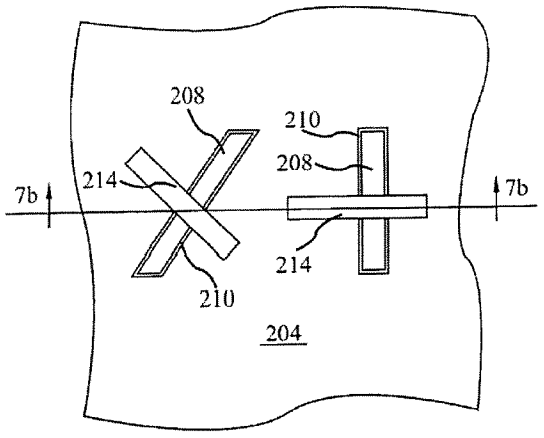
Applicants respectfully traverse the 35 U.S.C. § 102(b) rejection of claims 1-3, 5-6, and 9-13 as allegedly being anticipated by Fried. As set forth in detail below, Fried does not teach, disclose or suggest a gate insulator which covers at least two different crystal planes. Accordingly, the Section 102 rejection is respectfully traversed.

Applicants' claim 1, as amended, recites:

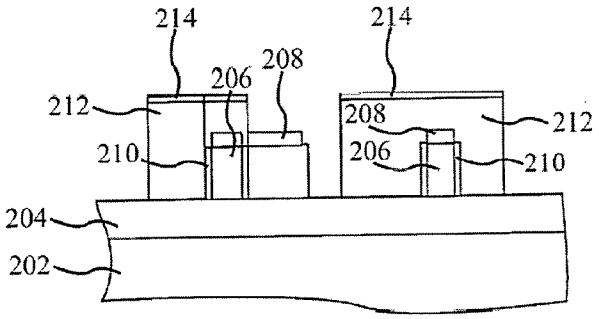
> 1. A MIS transistor, comprising:
>
> a semiconductor substrate comprising a projecting part of which surfaces are at least two different crystal planes on a principal plane;
>
> a gate insulator for covering at least a part of each of said at least two different crystal planes constituting the surface of the projecting part;
>
> a gate electrode comprised on said at least a part of each of said at least two different crystal planes constituting the surface of the projecting part so as to be electrically insulated therefrom by the gate insulator; and
>
> a pair of diffusion regions having the same conductivity type and formed on both sides of the gate electrode in the projecting part so

as to face said at least a part of each of said at least two different crystal planes constituting the surface of the projecting part.

Fried is directed to the design and fabrication of complementary metal oxide semiconductor (CMOS) fin field effect transistors (FinFETs) on the same substrate utilizing various crystal planes for FET current channels. [Fried, ¶0011]. In one embodiment, as shown by the top and cross-sectional views depicted in Figs. 7a and 7b, respectively (reproduced below), Fried discloses a typical structure for a CMOS FinFET fabricated from a semiconductor layer (206) situated on a buried insulator layer (204) which, in turn, is supported by a substrate (202). The fins are formed by anisotropically etching the semiconductor layer (206) after depositing and patterning a hard mask (208). A gate insulator layer (210) is then formed on the opposing vertical sidewalls and end walls of the fins. Gate structures are formed by depositing and patterning a gate conductor layer (212) using a second hard mask film (214). [Fried, ¶0057].



[Fried, Fig. 7a].

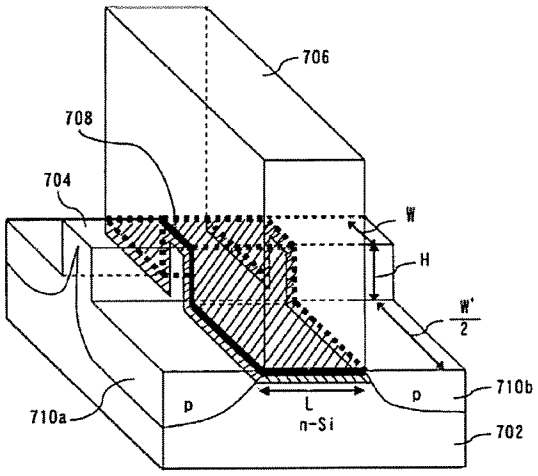


[Fried, Fig. 7b].

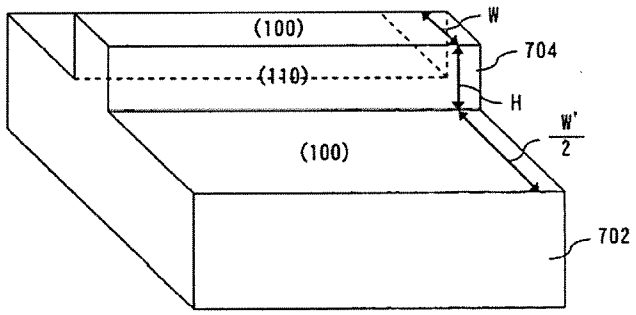
The Office Action contends that Fried's gate insulator layer (210) corresponds to Applicants' gate insulator for "covering at least a part of each of said at least two different crystal planes" as recited in pending claim 1. [11/16/07 Office Action, p. 5]. However, Fried's gate insulator layer (210) only covers the vertical sidewalls of the projecting fins, thereby

covering a single type of crystallographic plane (e.g., the {001} planes). The upper surface of each fin is not covered by the gate insulator (210), but rather is covered by a hard mask (208).

Applicants, on the other hand, are directed to a metal insulator semiconductor (MIS) transistor wherein the gate insulator covers at least two different crystal planes as shown, for example, by Figs. 6 and 7 below. Figure 7 shows that the projecting portion (704) is formed with the (100) plane as its upper surface and (110) planes as its side surfaces. In Fig. 6, each plane (e.g., the {100} and {110} planes) of the projecting portion (704) is covered with an insulating layer (708) and a gate electrode (706). A comparison of Applicants' Figs. 6-7 with Fried's Figs. 7a-b shows that Fried's insulator layer is not formed on at least two different crystal planes. Furthermore, Applicants respectfully note that Fried's fins (or projecting portions; 206 and 212) are formed on a buried insulator (204) as opposed to directly on the semiconductor substrate (202). As such, Fried's structures are not formed from a "semiconductor substrate comprising a projecting part" as recited in Applicants' claim 1.



[Applicants, Fig. 6].



[Applicants, Fig. 7].

Accordingly, Fried fails to teach, disclose, or suggest a MIS transistor including a "semiconductor substrate comprising a projecting part of which the surfaces are at least two

different crystal planes" and a "gate insulator for covering at least a part of each of said at least two different crystal planes constituting the surface of the projecting part" as recited in Applicants' amended claim 1. Applicants respectfully submit that claim 1 is patentably distinct from Fried for at least this reason. Independent claim 5 recites a MIS transistor which also encompasses this same patentable subject matter and, as such, is asserted to be allowable for at least similar reasons. Since claims 2-3, 6, and 9-13 depend either directly or indirectly from claims 1 and 5 they are all allowable for the same additional independent reasons. Applicants respectfully request withdrawal of the Section 102(b) rejection and assert that all pending claims are now allowable and early, favorable action in that regard is requested.

Applicants have chosen in the interest of expediting prosecution of this patent application to distinguish the cited documents from the pending claims as set forth above. These statements should not be regarded in any way as admissions that the cited documents are, in fact, prior art. Furthermore, Applicants have not specifically addressed the rejections of the dependent claims. Applicants respectfully submit that the independent claims, from which they depend, are in condition for allowance as set forth above. Accordingly, the dependent claims also are in condition for allowance. Applicants, however, reserve the right to address such rejections of the dependent claims in the future as appropriate.

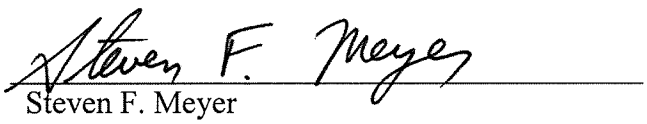
CONCLUSION

For the above-stated reasons, this application is respectfully asserted to be in condition for allowance. An early and favorable examination on the merits is earnestly solicited. In the event that a telephone conference would facilitate the examination of this application in any way, the Examiner is invited to contact the undersigned at the number provided.

THE COMMISSIONER IS HEREBY AUTHORIZED TO CHARGE ANY ADDITIONAL FEES WHICH MAY BE REQUIRED FOR THE TIMELY CONSIDERATION OF THIS AMENDMENT UNDER 37 C.F.R. §§ 1.16 AND 1.17, OR CREDIT ANY OVERPAYMENT TO DEPOSIT ACCOUNT NO. 13-4500, ORDER NO. 5000-5291.

Respectfully submitted,
MORGAN & FINNEGAN, L.L.P.

Dated: March 17, 2008

By: 
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